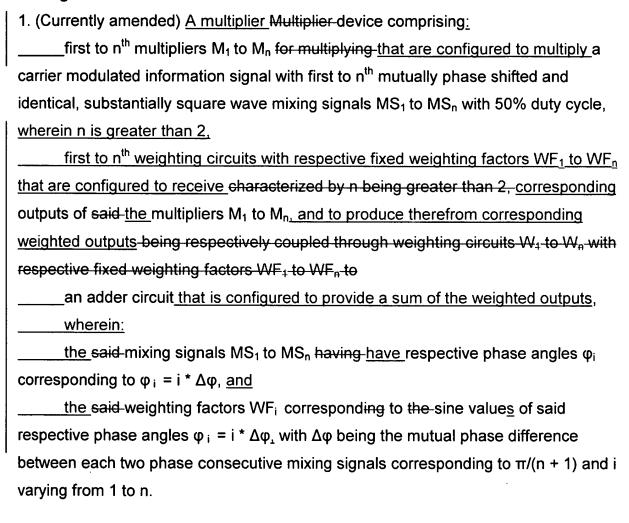
Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

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2. (Currently amended) <u>Multiplier The multiplier</u> device according to <u>of claim 1</u>, eharacterized by <u>wherein n corresponding corresponds</u> to (N+1)/2 for an elimination of all harmonics up to the Nth order from the <u>an</u> output of <u>said the</u> adder circuit. 3. (Currently amended) <u>Multiplier The multiplier</u> device according to <u>of</u> claim 1-or 2, eharacterized by said-wherein the mixing signals MS₁ to MS_n being <u>are</u> derived from a local oscillator signal with frequency fo through an arrangement of fixed phase shift means and/or frequency divider means.

4. (Currently amended) Multiplier The multiplier device according to of claim 3,
characterized by including:
a local oscillator circuit, and supplying an oscillator signal with frequency fo to
a serial arrangement of first to n th phase shifting means shifters that is
configured to receive an oscillator signal with frequency fo from the local oscillator
circuit, each phase shifter providing a fixed phase shift of $\Delta \phi$ and supplying
respectively mixing signals MS_1 to MS_n to said-the first to n^{th} multipliers M_1 to M_n .
5. (Currently amended) Multiplier The multiplier device according to of claim 4,
characterized by said wherein the local oscillator circuit generating-includes:
an oscillator that is configured to provide a clock control signal with clock
frequency n * fo, being supplied through
a frequency divider with dividing factor n that is configured to receive the clock
control signal and to provide a frequency divided output signal to said the serial
arrangement of first to n th phase shifting means shifters, each phase shifter of said
first to nth phase shifting means comprising including a D-flip-flop being that is clock
controlled by said the clock control signal and providing said to provide the fixed
nhase shift of Λω

6. (New) The multiplier device of claim 3, including

a plurality of fixed phase shift devices that are configured to receive the local oscillator signal and provide therefrom the mixing signals.

7. (New) The multiplier device of claim 3, including

a plurality of frequency dividers that are configured to receive the local oscillator signal and provide therefrom the mixing signals.

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- 8. (New) The multiplier device of claim 2, wherein the mixing signals MS₁ to MS_n are derived from a local oscillator signal with frequency fo.
- 9. (New) The multiplier device of claim 8, including

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a plurality of fixed phase shift devices that are configured to receive the local oscillator signal and provide therefrom the mixing signals.

10. (New) The multiplier device of claim 10, including

a plurality of frequency dividers that are configured to receive the local oscillator signal and provide therefrom the mixing signals.

11. (New) The multiplier device of claim 8, including

a local oscillator circuit, and

a serial arrangement of first to n^{th} phase shifters that is configured to receive an oscillator signal with frequency fo from the local oscillator circuit, each phase shifter providing a fixed phase shift of $\Delta \phi$ and supplying respectively mixing signals MS₁ to MS_n to the first to n^{th} multipliers M₁ to M_n.

12. (New) The multiplier device of claim 11, wherein the local oscillator circuit includes:

an oscillator that is configured to provide a clock control signal with clock frequency n * fo, and

a frequency divider with dividing factor n that is configured to receive the clock control signal and to provide a frequency divided output signal to the serial arrangement of first to n^{th} phase shifters, each phase shifter including a D-flip-flop that is clock controlled by the clock control signal to provide the fixed phase shift of $\Delta \phi$.